Adi Shankara
INSTITUTE OF ENGINEERING AND TECHNOLOGY
Ph: 0484-2463825
Email: info@adishankara.ac.in
Website: www.adishankara.ac.in

NBA NATIONAL BOARD OF ACCREDITATION

DEPARTMENT OF ELECTRONICS AND COMMUNICATION

EXPLORE, DREAM, DISCOVER

ISSUE 54 MONTHLY NEWSLETTER AUGUST 2022

GENESIS

IGNITING THOUGHTS

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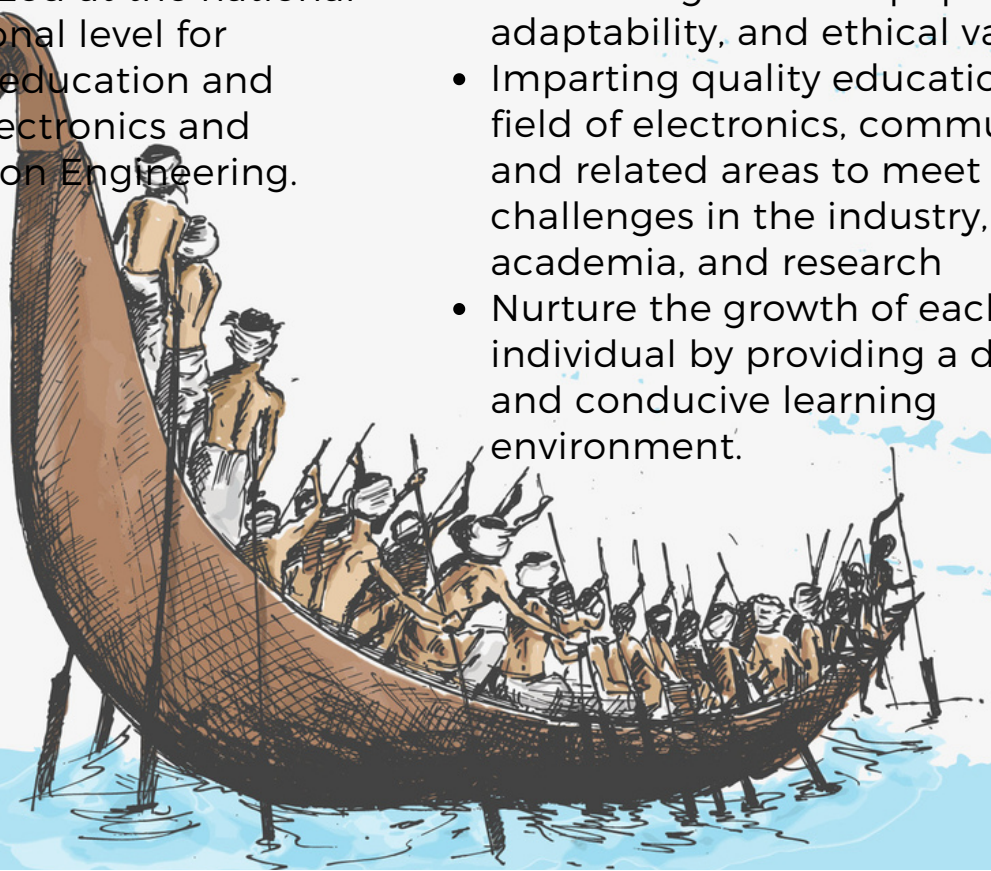
Contents

Vision

- To be recognized at the national and international level for excellence in education and research in Electronics and Communication Engineering.

Mission

- Inculcating leadership qualities, adaptability, and ethical values
- Imparting quality education in the field of electronics, communication, and related areas to meet the challenges in the industry, academia, and research
- Nurture the growth of each individual by providing a dynamic and conducive learning environment.



NBA ACCREDITION

Department of Electronics and Communication Engineering got re-accredited by the National Board of Accreditation (NBA) for Academic Years 2022-23, 2023-24, 2024-25; upto 30/06/2025.

CONGRATULATIONS TO UNIVERSITY TOPPERS ON EXEMPLARY RESULTS IN KTU EXAMINATIONS (2018-2022 BATCH ECE)

AISHA MEHRIN K.I
CGPA - 9.09

PARVATHI S KUMAR
CGPA - 9.07

MALAVIKA J
CGPA - 9.03

DIVYA D MENON
CGPA - 8.96

AUSTIN JOSE
CGPA - 9.00

VARSHA T.R
CGPA - 8.85

SAMAVARTHANA 2022 - GRADUATION CEREMONY

The graduation ceremony for the students passed out in 2022 was conducted on 20th August 2022. The chief guest for the event was Sri. A C K Nair, Former Airport Director, CIAL. The function began with the welcome address by Dr. Suresh Kumar V, Principal, ASIET followed by the Presidential address by Sri. K Anand, Managing Trustee, Adi Sankara Trust. Ms.AISHA MEHRIN K I & Ms. PARVATHY S KUMAR received the award for class toppers. Ms. HRIDAYA U MALLIA received the best outgoing student award.


HRIDAYA U MALLIA
ACHIEVEMENTS
Crystal


CGPA:9.07
Crystal

ECE Batch of 2018-22

PLACEMENTS AFTER ECE

HAPPY NEWS

FUNDING FROM KTU FOR FDP - ALBINS & ARYA PAUL

APJ Abdul Kalam Technological University has sanctioned an amount of Rs.200,000 for the proposal to conduct a Faculty Development Programme on " Deep Learning & ML Applications in Computer Vision", from 12th December to 16th December 2022. This FDP focuses on providing an introduction to the impacts of Deep learning and AI on CV applications. The FDP intends to disseminate knowledge in the domain of Computer Vision, ML, and Deep Learning. It empowers the participants to innovate and improve business processes with the help of AI/ML. The coordinators for the FDP are Mr. Albins Paul and Ms. Arya Paul, Assistant Professor, Department of ECE.

INDUSTRY ORIENTED PROJECT- BEACON ENERGY STORAGE SYSTEMS, Pvt. Ltd

Proud to announce that ECE students along with EEE students successfully completed the project titled " Inverter and BMS Data Monitoring using WiFi" in association with Beacon Energy Storage Systems Pvt. Ltd. They were funded Rs. 15000 by the industry after the final demonstration.

MINI PROJECT EXHIBITION

The mini-project evaluation and an exhibition of 2019-23 batch students were conducted at the project lab on 01/08/2022. Students exhibited their projects and were evaluated by a team of senior faculty members.

CONGRATULATIONS

Nirmal V Babu
S6 EC-B

Congratulations to Nirmal V Babu 2019-23 EC B batch for bagging first prize in 2 Day Idea pitching competition IDEATE.

MORE PLACEMENTS

Aparna Mohanan (MTech VLSI and Embedded systems) Placed in HCL.

Congratulations to Mr. JAYESH T P for getting Ph. D admission in KALASALINGAM University, Tamil Nadu

FAREWELL

2020-2022 M.TECH BATCH

2018-2022 BATCH B .TECH

FAREWELL - Dr. Prameela B

As you move into a new venture may luck and success be with you always. Thank you for being a great colleague and we miss you Ma'am

TECH TALKS

STAFF ZONE

Spin Transfer Torque Random Access memory (STT-MRAM): Future Memory Technology

Mrs. Aswathi Assistant Professor, Department of ECE.

Memory is one of the most important defining components used in every computer system, storage solution, and mobile device in existence today. Performance, scalability, reliability, and the raw cost of memory are major criteria in determining the economic success or failure of each system product brought to market. Nearly all of today's products use one or a combination of charge-based, volatile memories, DRAM and SRAM, and non-volatile memories NOR and NAND flash. These existing memories have significant advantages that led to market dominance over the last 30 years. They also come with drawbacks that cloud their future, since systems consistently need to be faster, smaller, more reliable, and less expensive to compete effectively over the next five to ten years. There are new disruptive technology challengers coming into the market, specifically non-volatile memories (NVM) such as resistive RAM (RRAM) and phase-change RAM (PCRAM) that promise high performance, low power consumption, and unlimited endurance. Magnetic RAM (MRAM) is one of these emerging technologies. MRAM has been in development since the 1990s, and several companies have introduced production devices. With MRAM, a memory cell is comprised of a magnetic tunnel junction (MTJ), which has been widely used as read head for hard-disk drives for many years. STT-MRAM is the latest design in the non-volatile magnetic RAM (MRAM) family. The information storage in STT-MRAM is a Magnetic Tunnel Junction (MTJ) instead of electric charges, which makes the difference between it and conventional RAM.

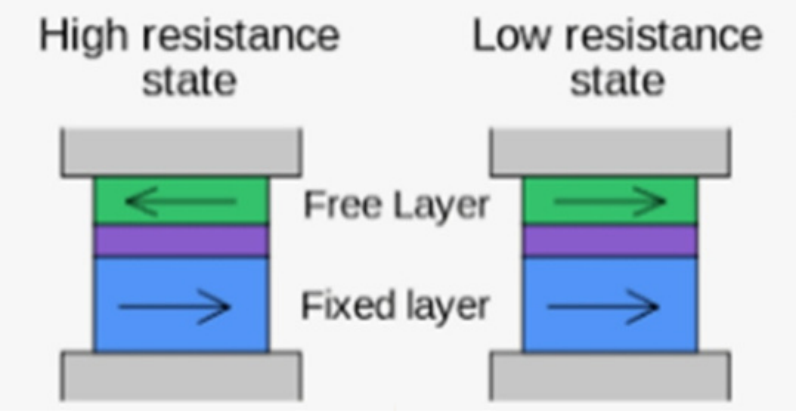


Fig1. MTJ logic state representation

Each MTJ contains two ferromagnetic layers and one tunnel barrier layer. One of the ferromagnetic layers (fixed layer) has fixed magnetic direction while the other one (free layer) can change its magnetic direction by an external electromagnetic field or a spin transfer torque. In case the two ferromagnetic layers have different directions, the MTJ resistance is High indicating a “Logic 1” state. If the two layers have the same direction, the MTJ resistance is Low, indicating a “Logic 0” state. Early MRAM devices utilized in-plane MTJ (iMTJ) where the magnetic moments (a vector having a magnitude and direction) stay parallel to the substrate silicon surface. There is now another, more-optimized version of MTJ, called perpendicular MTJ (pMTJ), where the magnetic moments are perpendicular to the silicon substrate surface. While the iMTJ-based STT-MRAM does not scale well below 90nm nodes and is not cost competitive on 200mm wafers, the pMTJ-based STT-MRAM scales extremely well, down to below 10nm. It is expected to be cost-competitive with other memory technologies, such as DRAM. This scalability enables STT-MRAM to become the viable alternative for DRAM and flash in low- and medium-density applications over the next few years.

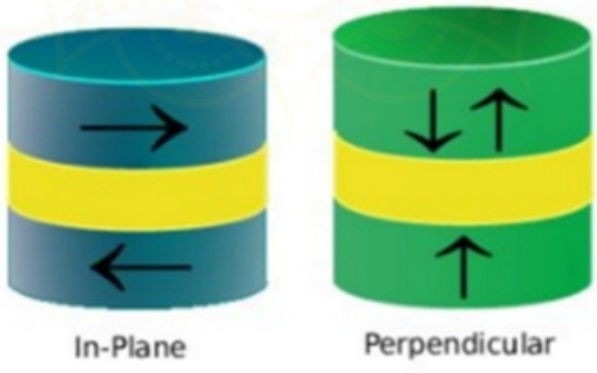


Fig2. In-plane MTJ and Perpendicular MTJ

STT-MRAM Basics

A typical STT-MRAM bit cell consists of an MTJ connected in series with an nMOS transistor between a bit line (BL) and a source line, named 1T1MTJ cell structure, as shown in Fig. 3. The MTJ is used as a storage element, while the transistor acts as an access device controlled by a word line (WL).

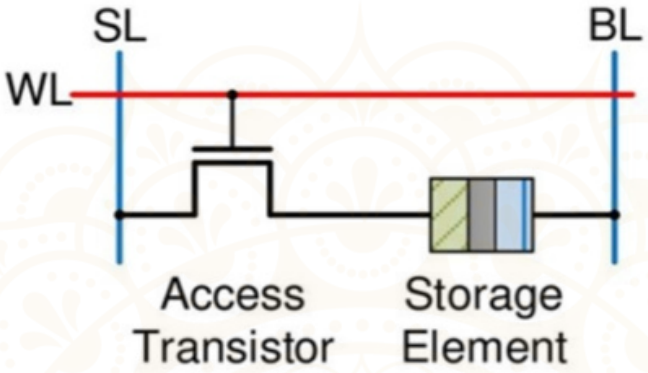
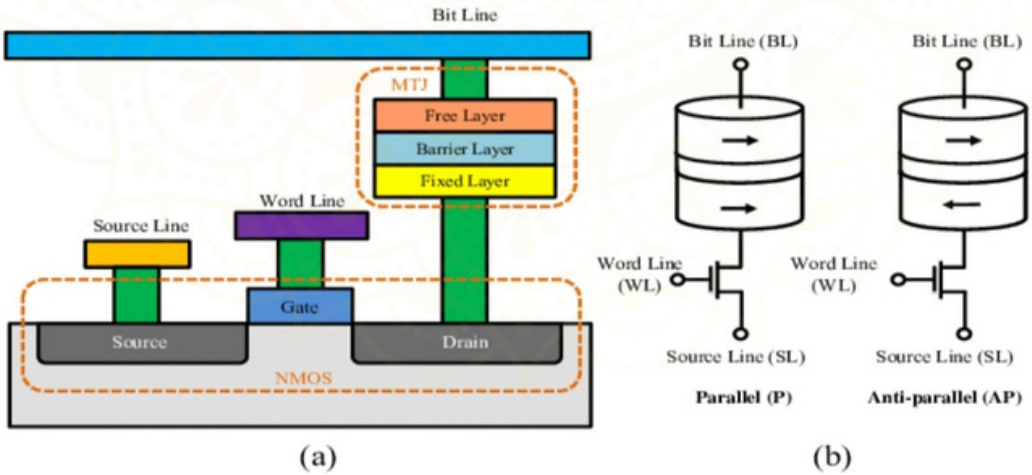


Fig3. 1T-1 MTJ Cell

Read Operations: Read operation begins when the wordline (WL) is selected and a voltage is applied between the bit-line (BL) and the source-line (SL). Current will pass through the MTJ or not depending on the state of the MTJ which can be sensed/measured.



(a) STT-RAM cell, and (b)its equivalent circuit

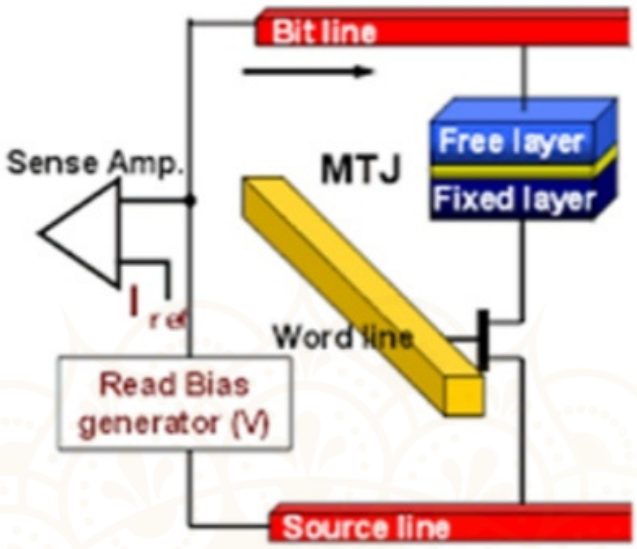


Fig 4. Read circuitry

Write Operations: Write operation begins when the WL is selected and a positive voltage difference is established between SL and BL for writing"Logic 0" or a negative voltage difference is established to write a "Logic 1". The current amplitude required to ensure a successful write is related to the material of the tunnel barrier layer, the writing pulse duration, and the MTJ geometry.

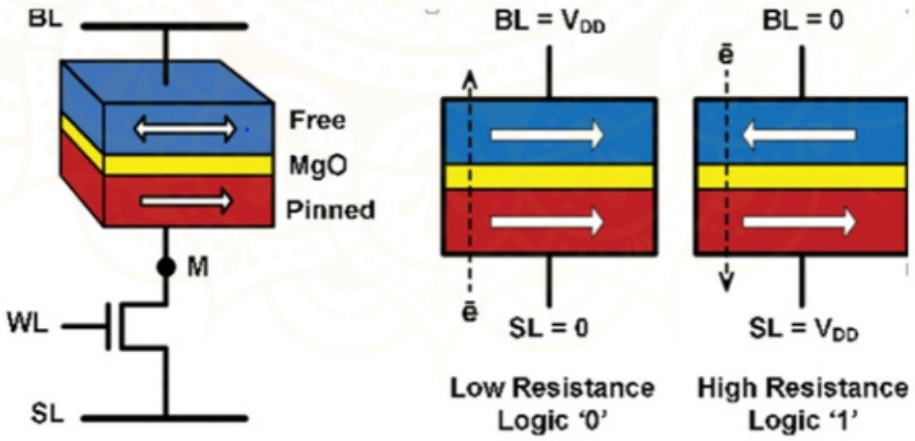


Fig5. Write logic 0 and 1

Applications

As a discrete memory device, STT-MRAM is being used as a replacement for SRAM, DRAM, and NOR-flash due to its higher speed, lower latency, scalability, and unlimited endurance. STT-MRAM does not require a power-refresh like DRAM, and the read process is not destructive. This situation provides a significant power advantage, as well as lower latency at the system level.In many of today's SOCs, CPUs, and GPUs, between 50% and 80% of the die-area is consumed by memory. This embedded memory tends to be mostly SRAM using four or six transistors. In comparison, STT-MRAM uses one transistor. Recent CPUs have also shown the incorporation of e-DRAM to save die-size, in spite of its being a very difficult process. STT-MRAM, with ease of integration due to standard CMOS, is ideally suited for such applications. It provides a significant die-size reduction while providing high-speed NVM close to the logic. This is expected to provide a lower cost, a faster boot time, and a number of new functionalities, especially for mobile and storage devices.Enterprise storage is the major application fit for pMTJ-based STT-MRAM. Storage arrays and datacenters are undergoing a dramatic change from old legacy HDD-based systems to all-silicon (solid state drive, SSD) flash-based systems.

	SRAM	DRAM	Flash (NOR)	Flash (NAND)	FeRAM	MRAM	PRAM	STT-RAM
Non-volatile	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Cell Size (F^2)	50-120	6-10	10	5	15-34	16-40	6-12	6-20
Read Time (ns)	1-100	30	10	50	20-80	3-20	20-50	2-20
Write/Erase Time (ns)	1-100	50/50	1µs/ 10ms	1ms/ 0.1ms	50/50	3-20	50/120	2-20
Endurance	10^{16}	10^{16}	10^{5}	10^{5}	10^{12}	$>10^{15}$	10^{10}	$>10^{15}$
Write power	Low	Low	Very high	Very high	Low	High	Low	Low
Other power consumption	Current leakage	Refresh current	None	None	None	None	None	None
High voltage required	No	2V	6-8V	16-20V	2-3V	3V	1.5 – 3V	<1.5V
	Existing products						Prototype	

Table 1. Comparison of various memory technologies

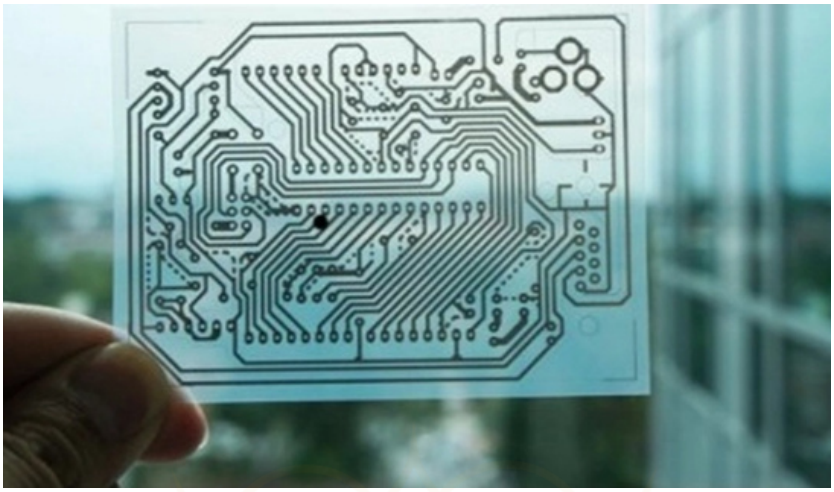
In conclusion, the above table shows comparison of existing and upcoming memory technologies. Each device has its advantages and disadvantages. Current generation flash memory is increasingly limited by its cycle endurance. High voltage is required to write and erase flash memory, and the write power is very high. Ferroelectric memory solves the "high voltage" and "write power" issue, but falls short on endurance. MRAM has a high endurance level, but the write power becomes worse as the devices scale down. Phase-change memory has low write power, but is somewhat limited in endurance. STT-RAM shows the most promising characteristics to become an Universal Memory in future having high speed as that of SRAM, high density as that of DRAM and non-volatile as FLASH.

STUDENT ZONE

Printed Electronics

Ms. SEREEN SABU, S4 ECB

The printed electronics technology is a novel way to manufacture electronics, using standard graphic arts printing processes, such as screen printing, flexography and inkjet printing and various types of electronic devices and circuits can be fabricated on unconventional substrates. Almost any material can be used for this purpose - plastic, textiles ,paper and nanomaterials are some good examples of such surfaces. Nanomaterials are widely pursued since they offer numerous advantages in terms of ease of processing, good compatibility with a variety of substrates, and great opportunity for structural modifications.



Printing Technology

Printing technologies divide between sheet-based and roll-to-roll-based approaches. Sheet-based inkjet and screen printing are best for low-volume, high-precision work. Gravure, offset and flexographic printing are more common for high-volume production.

Types of Printing Technology

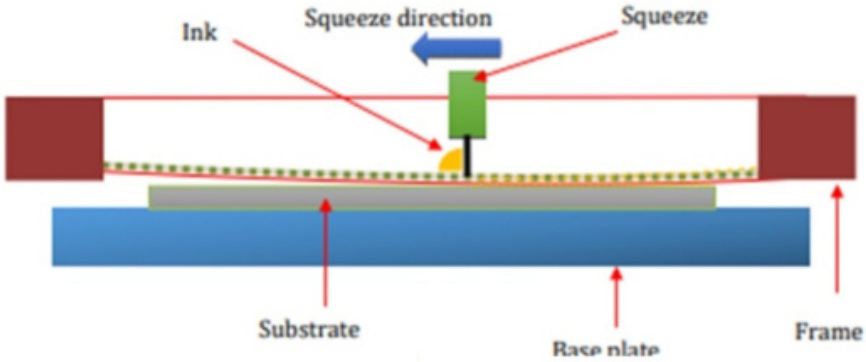
1. Inkjet Printing

The main advantage of an inkjet printing process is the no need for a physical mask or image carrier. Instead, inkjet printing uses a direct deposition technique and a virtual digital image carrier. Inkjet printing is known for thin ink deposits and is classified into either continuous inkjet or drop-on-demand inkjet based on the ink transfer method used. Drop-on-demand inkjet is further categorised as thermal inkjet and piezo inkjet printing processes.

2. Screen Printing

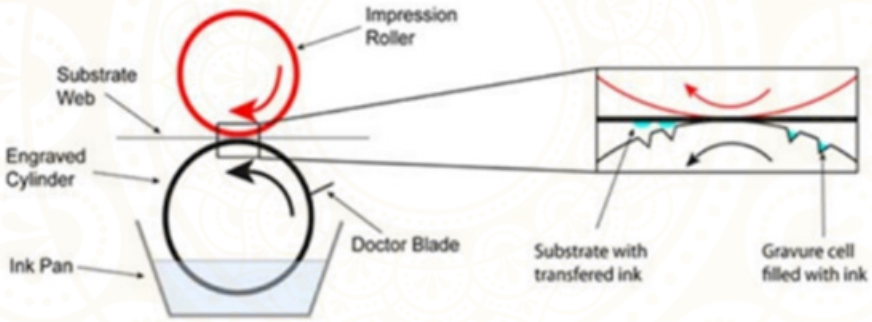
Screen printing uses a porous mesh image carrier (screen), yielding thicker ink deposits than other printing methods. The typical screen printing process is shown in the figure. A squeegee and screen printing plate are the main components of the screen printing process. A screen printing plate consists of screen fabrics, stencils, and frames.

The materials used for the screen fabric and stencil vary depending upon the use of solvents and cleaning agents. Polyurethane is the usual material used for the squeegee. Ink is applied on top of the screen. The squeegee is used to sweep the ink on top of the screen with pressure.The ink passes through the screen and transferred onto the substrate which typically has the form of a single sheet .



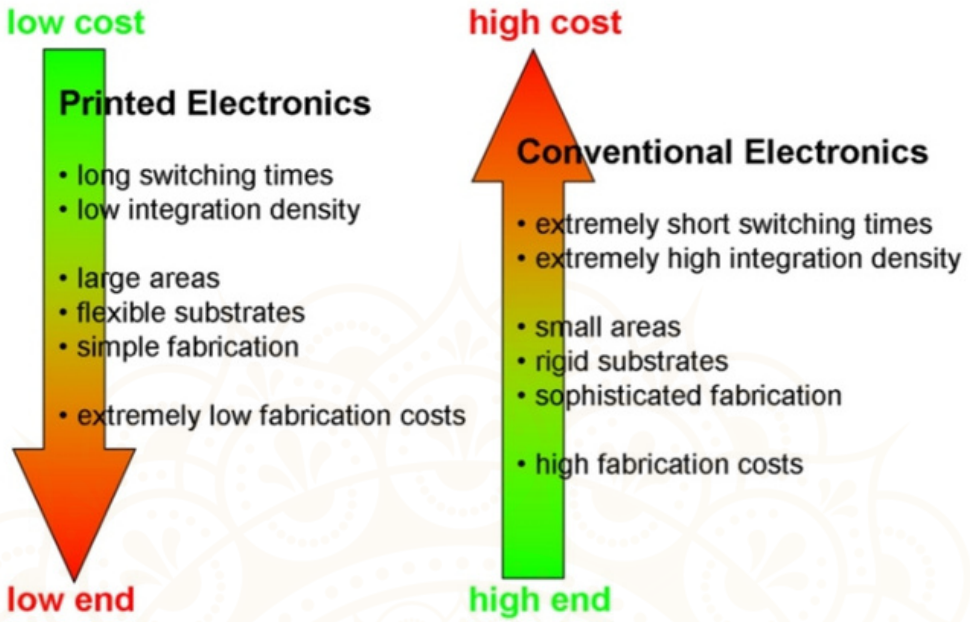
3. Gravure Printing

Gravure printing is known for its high print quality, high print speeds, variable film thickness, use of low viscosity inks, and simplicity of transferring the ink onto the substrate.The gravure cylinder (image carrier), doctor blade, impression roller, and ink fountain are the main components of the typical gravure printing process



4. Flexographic Printing

Flexographic printing is known for depositing a wide range of thicknesses with the same resolution. A flexographic print is made by creating a positive mirrored master of the required image as a 3D relief in a rubber or polymer material.



Printable materials have potential applications at all levels of microelectronics. Printing processes have several advantages such as selective deposition, repair, and re-print capability. Printed electronics are in use or under consideration include wireless sensors in packaging, skin patches that communicate with the internet, and buildings that detect leaks to enable preventative maintenance. Most of these applications are still in the prototyping and development stages.

STAFF ACHIEVEMENTS

Dr. V T Gopakumar. Professor

- Participated in Fully funded 'Innovation School' in person program organized by the OPTICA Foundation (formerly Optical Society of America, OSA)) in Washington D C, have got honorable mention from judges and pivot prize from the audience for our pitch 'Command Clean' on 10th June to 16th June at Optica foundation in Washington D C
- Participated in Faculty Development Program(FDP) “Designing and Modelling of IoT, AI & ML Systems” from 1st August to 5th August 2022 on AICTE, Arm Education, STMicroelectronics, with support from Microsoft and NIELIT Calicut

Dr. Prameela B, Associate Professor

- Dr. Prameela B and Sukanya M G Published a paper titled "Mixer Design for Global Navigation Satellite System" in Grenze International Journal of Engineering and Technology
- Dr.Prameela B and Hridaya U Mallia presented a paper titled " Complex IF filter for GNSS applications" in IEEE sponsored ICNGIS 2022
- Dr Prameela B and M G Sukanya Published a chapter titled "Mixer Design for Global Navigation Satellite System" in the proceedings of SRISHTI 2022 with ISBN ISBN- 978-93-5680-852-2

Mr. Prajeesh P A, Assistant Professor

- Participated in Faculty Development Program(FDP) on Advanced micro/Nano sensor technologies from 18/7/22 to 20/7/22 organized by Dept of ECE, Government engineering College,Palakkad

Mrs. Neema M, Assistant Professor

- Participated in Faculty Development Program(FDP) on Advanced micro/nano sensor technologies from July 18 to 20 organized by GEC Palakkad

Mrs. Divya V Chandran, Assistant Professor

- Completed an online course Create Your First Python program From UST on August 6,2022 by Coursera

Mrs.Aswathy N, Assistant Professor

- Participated in Faculty Development Program(FDP) on Advanced Materials and Process for Next-Generation Nanoelectronic Devices:Challenges and Opportunities from 27th june to 4th july 2022 organized by SRM Institute of Science and Technology, Chennai.

STUDENTS ACHIEVEMENTS

Name	Title of Course/Activity attended	Conducted By
ANAL C D	Webinar on " Introduction to AR/VR "	IIC & IEI
	CHAKARAVYUHA 21	BHS DEPARTMENT
	Python	SkillVertex
	Autom8 Home automation workshop	IEEE SB ASIET
ALBIN PAUL	IEI WEBINAR	Ece
NOEL MARTIN	Python and data visualization	Devtown
SREELAKSHMI P M	Blood donation camp	Nss
FATHIMA MUHSINA VA	Boot camp for basics for web development	Devtown
FATHIMA MUHSINA VA	Basics of web development	Google microsoft
JAISON T POULOSE	Selected for the finale round of 30 hour hackathon HackaversuMM'22	MMDU, Harayana
	Selected as Google Developer Student Club Lead	Google Developers Club
AKESHA SANAL S.S	Cybersecurity and ethical hacking	IEI

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