Workshop on

Recent Trends in VLSI Technology

We, Department of Electronics & Communication Engineering, are conducting a sponsored Faculty Development Program (FDP) titled "Workshop on Recent Trends in VLSI Technology" from 3rd January to 7th January 2017.

This FDP focuses on the recent trends in VLSI technology with an emphasis on current research avenues. It intends to provide opportunity for participants to interact with experts from both academics and industry. Hands on sessions will be beneficial to the faculty members teaching VLSI related courses in various PG programs and research scholars working in this field.

About the Institute
Ideally located in an idyllic ambience, the Institution kindles vibrant memories of the serene presence of Jagadguru Adi Shankara. Affiliated to A.P.J Abdul Kalam Technological University and approved by AICTE. ASIET is the first self financing technical education centre to be awarded the ISO 9001:2008 certification. Established in 2001 and aptly run by the Sringeri Mutt with the benign blessings of Sree Sree Bharathithreetha Mahaswamigal, ASIET boasts a state of new dimensions of spirituality and education. Adi Shankara Institute of Engineer-ing & Technology was established at Kalady with the aim of providing value added technical excellence and ethical values. The college is run by Adi Shankara Trust.

About the Department
The Department of Electronics and Communication Engineering, with well qualified and experienced faculty technical staff and students, is committed to be a center for excellence in education and research. The department offers B.Tech in ECE and M.Tech in VLSI and Embedded Systems engineering and Communication Engineering. The department has well equipped labs to facilitate research and consultancy in the area of VLSI, Signal Processing and communication
Course Objective:
The advances in VLSI technology have lead to a state where dependence of human life on semiconductor technology is ubiquitous. This work-shop focuses on the recent trends in VLSI technology with an emphasis on current research avenues. It intends to provide opportunity for participants to interact with experts in this field from both academics and industry. Hands on sessions will be beneficial to the faculty members teaching VLSI related courses in various PG programs.

Course Content:
- Design – low power, SoC, 3D IC Analog/RF
- Verification and timing
- VLSI system testing
- Semiconductor device modelling
- Algorithm Implementation on FPGA
- Hands-on experience of
- Analog CMOS circuit design and layout using Cadence Virtuoso
- FPGA Programming using VIVADO

Click here to view the Program Schedule

Resource Persons:
1. Dr. Amit Acharya, IIT Hyderabad.
2. Mr. Praveen Kumar, Wipro Technologies.
3. Dr. Jobymol Jacob, Model Engineering College, Ernakulam.
4. Dr. S. Krishna Kumar, Federal Institute of Science and Technology, Ernakulam.
5. Dr. S Rajaram, Thiagarajar College of Engineering, Madurai.
6. Dr. Ramkumar S, Muthoot Institute of Technology, Ernakulam.
7. Mr. Jagadeesh Kumar P, College of Engg., Cherthala.
Targeted audience:
Faculty members interested in VLSI, Research Scholars and PG students in the field of VLSI can apply.

Fee Details:
Faculty Members: 1500/
Students: 750/

How to Apply
Confirm your participation by submitting the Google Form ([https://goo.gl/forms/o0aJAfvgGfFTiDwBa2](https://goo.gl/forms/o0aJAfvgGfFTiDwBa2)) on or before 26/12/2016. The registration form recommended by the Head of the Institution has to be submitted in person on first day of the programme.

Mode of Payment:
Registration fee is to be paid by cash/ NEFT. If payment is done through NEFT, submit the payment receipt on first day of the programme.

Name of Bank: Vijaya Bank
A/C No:209201011000413
IFSC : VIJB0002117

Note:
☐ The registration will be done on first come first serve basis.
☐ Maximum numbers of participants are restricted to 40.
☐ The registered participants will be provided boarding and lodging in the institute campus at nominal rates if requested.

Convener:

Prof. N. Hariharan (Dean, PG Studies)
Coordinators:

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CLICK HERE TO REGISTER